REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comment regarding this burden estimates or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Services. Directorate for information Operations and Reports. 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	10/30/98	Progress - 1/1/98-10/30/98

4. TITLE AND SUBTITLE
Silicon-Based On-Wafer Packaging for High Isolation in High-Density Circuits

5. FUNDING NUMBERS
N00014-95-1-0546

6. AUTHOR(S)
Linda P.B. Katehi

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Michigan, Ann Arbor
Dept. Electrical Engineering and Computer Science
1301 Beal Avenue
Ann Arbor, MI 48109-2122

8. PERFORMING ORGANIZATION REPORT NUMBER
033095-2-T

9. SPONSORING / MONITORING AGENCY NAMES(S) AND ADDRESS(ES)
Office of Naval Research
Program Officer William J. Stachnik ONR313
Ballston Centre Tower One 800 North Quincy Street
Arlington, VA 22217-5660

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)
This project concentrates on the development and demonstration of a novel approach which is appropriate for the development of circuits that require high isolation and high density of integration. In the past ten months, we have extensively investigated the development of a vertically integrated circuit configuration with emphasis on understanding cross talk in various architectures in an effort to minimize it while at the same time circuit efficiency is optimized. The developed architectures for maximum isolation and minimum loss are presently applied towards the design of a three-stage low-noise amplifier. With the successful completion of this LNA (expected by the end of November) we will successfully move towards the development of a K/Ka-Band SSPA/LNA amplifier pair with an isolation between the receiving and transmitting components of better than -80 dB. In both configurations, high isolation between the neighboring circuit components will be achieved by vertically integrating the individual components and by incorporating an effective on-wafer Si micromachined package to further isolate electromagnetically the MMIC components. The performance will be compared to the state-of-the-art to demonstrate excellent electrical response with low cost and high density.

14. SUBJECT TERMS

15. NUMBER IF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Semi-Annual Report

on

Silicon-Based On-Wafer Packaging for High Isolation in High-Density Circuits

by

Linda P.B. Katehi

The University of Michigan

October 1998

ONR Contract : N00014-95-1-0546

19981109 067

DTIC QUALITY INSPECTED 4

Contract Number: N00014-95-1-0546
Reporting Period: January 1998-October 1998
Participating Faculty: Linda P.B. Katehi
Participating Students (supported partially or fully during the reporting period:
Manos Tentzeris
John Papapolymerou
Rashaunda Henderson
Jim Becker

Publications published or submitted during the reporting period :

1. John Papapolymerou, Rhonda Drayton and Linda P.B. Katehi, ***Micromachined Patch Antennas***, IEEE Trans. on Antennas and Propagation, Vol. 46, No. 2, Febr. 1998, pp. 275-283.
2. Rhonda F. Drayton, Rashaunda M. Henderson and Linda P.B. Katehi, ***Monolithic Packaging Concepts for High Isolation in Circuits and Antennas***, in press in the IEEE Trans. on Microwave Theory and Techniques, Vol. 46, No. 7, pp. 900-906, July 1998.
3. George Ponchak, Emmanouil Tentzeris and Linda P.B. Katehi, ***Characterization of the Coupling Between Adjacent Finite Ground Coplanar (FGC) Waveguides***, in press in the International Journal of Microcircuits and Electronic Packaging.
4. Steve Robertson, Linda P.B. Katehi and Mehran Matloubian, ***K-Band Flip-Chip HEMT LNA with Si-Micromachined Conformal Packaging***, submitted to IEEE Transactions on Microwave Theory and Techniques.

Presentations during the reporting period:

1. George Ponchak, Donghoon Chen, Jong-Gwan Yook and Linda P.B. Katehi, ***Filled Via Hole Fences for Crosstalk Control of Microstrip Lines in LTCC Packages***, 1998 International Conference of Microelectronics and Advanced Packaging, San Diego, November 1998.
2. Linda P.B. Katehi and Gabriel Rebeiz, ***Micromachining Techniques for High-Frequency Circuits***, Proceedings of the 1998 URSI International Symposium, Atlanda, GA, June 1998.
3. R. Robertson, E.M. Tentzeris, T.J. Ellis and L.P.B. Katehi, ***Characterization of a CPW-MS Transition for Antenna Applications***, Proceedings of the 1998 International Symposium on Antennas and Propagation, Atlanda, GA, June 1998.
4. Jong-Gwan Yook and Linda P.B. Katehi, ***Suppression of Surface Waves Using Micromachining Techniques***, Proceedings of the 1998 International Symposium on Antennas and Propagation, Atlanta, GA, June 1998.
5. Rashaunda M. Henderson, Thomas A. Schwarz, Stephen Robertson, Linda P.B. Katehi, Michael Case and Mehran Matloubian, ***The Effects of Si-Micromachined On-Wafer Packaging on the Performance of K-Band Circuits***, Proceedings of the 1998 European Microwave Conference, October 1998, Netherlands.

Brief Description of Performed Research

This project concentrates on the development and demonstration of a novel approach which is appropriate for the development of circuits that require high isolation and high density of integration. This approach is based on silicon (Si) micromachining and can effectively provide on-wafer packaging for high quality, high-precision components that may be integrated in a three dimensional circuit configuration. The fabrication techniques required in this approach are compatible with standard IC processing and for this reason provide very low fabrication cost and very high precision. In the past ten months, we have extensively investigated the development of a vertically integrated circuit configuration with emphasis on understanding cross talk in various architectures in an effort to minimize it while at the same time circuit efficiency is optimized. The developed architectures for maximum isolation and minimum loss are presently applied towards the design of a three-stage low-noise amplifier. With the successful completion of this LNA (expected by end of November) we will successfully move towards the development of a K/Ka-Band SSPA/LNA amplifier pair with an isolation between the receiving and transmitting components of better than –80 dB. In both configurations, high isolation between the neighboring circuit components will be achieved by vertically integrating the individual components and by incorporating an effective on-wafer Si micromachined package to further isolate electromagnetically the MMIC components. The performance of the developed components will be compared in size and performance to the state of the art in order to demonstrate excellent electrical response in addition to very low cost and high density.

As it has been demonstrated by previous studies, microstrip lines printed on a 200μm Si substrate can couple by as much as -15 dB at 40 GHz when they are separated by 1mm. Finite ground coplanar waveguides show a better isolation. However, when they operate in an open environment their electromagnetic coupling cannot reduce to less than -40dB even when the lines separate by more than 1mm. On-wafer packaging can further reduce this coupling from -40 to -60dB without increasing the separation between the lines. Figures 1 and 2 show the various packaging mechanisms which have been investigated during this reporting period. Specifically, different line architectures have been investigated for W-band (Figure 1) and Ka-Band architectures (Figure 2). In all cases the line geometry was chosen to give a 50 Ohm impedance. The extension of the shielded CPW transmission line to a fully conformal integrated package involves the ability to shape the shielding cavity to follow the trace of the underlying CPW line on the surface of the MMIC. This is easily accomplished, since fabrication of the cavity is performed using lithographic and micromachining techniques

common to Si processing. The transmission line elements in a conformably packaged circuit are individually shielded, and circuit elements can be brought much closer than it is possible with open structures.

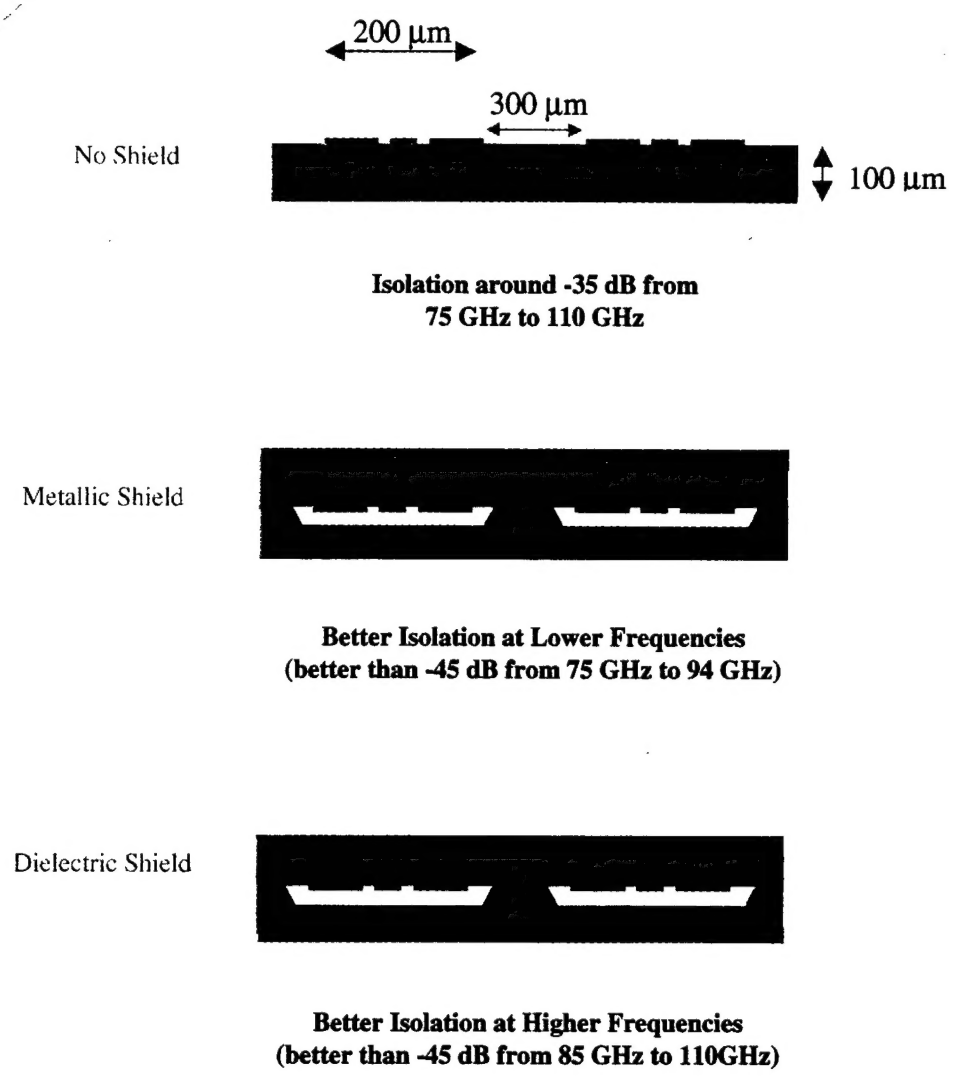
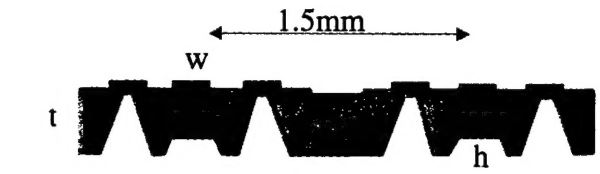
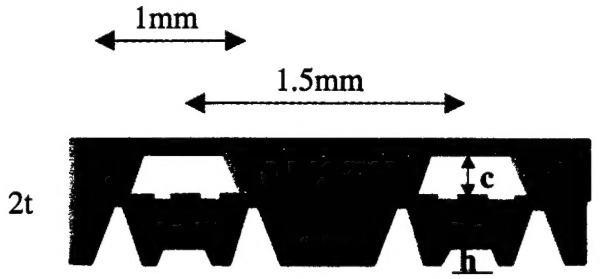


Figure 1: Line Architectures for W-Band Applications. Lines are separated by 300 microns and have a characteristic impedance equal to 50 Ohms.



Lower Shielding with Isolation from –60 dB at 5 GHz to –40 dB at 40 GHz



Complete Shielding with Isolation from –90 dB at 5 GHz to –50 dB at 40 GHz

Figure 2: Architectures for high isolation for Ka-Band applications. Lines are printed on 200micron Si high-resistivity wafers. The lines are separated by 1.5mm and are 1mm wide.

This study has led to the following conclusions:

- Coplanar waveguides lines of narrow cross section (less than 200 micron wide) exhibit high isolation even for small separation distances. When these lines are separated by 300 microns, maximum exhibited cross talk in W band is equal to –35 dB.

- To reduce this cross talk, the lines can be shielded on one side only by metallic or dielectric cavities. With this shielding, the cross talk reduces to values varying from –60 dB to –45 dB approaching the noise of the measurement set-up at the higher frequency range.

- To reduce this isolation further the lines have to be completely shielded. In this case

measurements has shown that the measured coupling is negligible (better than the noise of the measurement system).

- When these lines are separated by large distances (approaching 1 mm) isolation is better than - 60 dB and is rather independent of the shielding cavity for half shielded lines. Better isolation requires full shielding with metallized cavities.

- Metallized cavities while improve isolation, but at the same time they increase ohmic losses. For isolation around –60 dB, line geometries with dielectric shielding cavities are preferred since they combine high isolation with low loss.

- Lines with large cross section appropriate for low frequency applications tend to couple more when not packaged. Measurements have shown that when these lines are not shielded, isolation can be as low as –15 dB at 40 GHz. When these lines are packaged the coupling reduces to levels below the noise of the measurement system.

This novel integrated packaging approach has been applied to the three-stage Low-Noise Amplifier. Extensive results from this work are shown on the web site: ***http://copperharbor.engin.umich.edu/copy_of_onr/index.htm***. The study has indicated that on-wafer packaged single and three-stage amplifiers can produce very high-density, high-performance and low-cost circuits. This integration approach will be extended to a LNA/SSPA amplifier pair to demonstrate the development of a MMIC T/R module which is characterized by high stability in amplification and very high isolation between the receive/transmit functions of the unit. Both efforts will strive for the maximum possible density which will rely on a three dimensional integration.

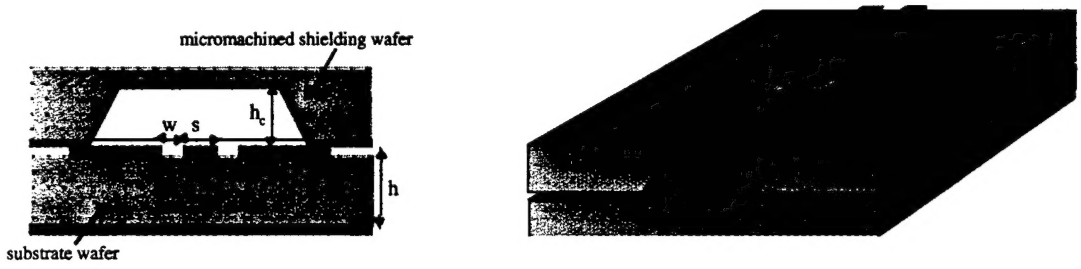
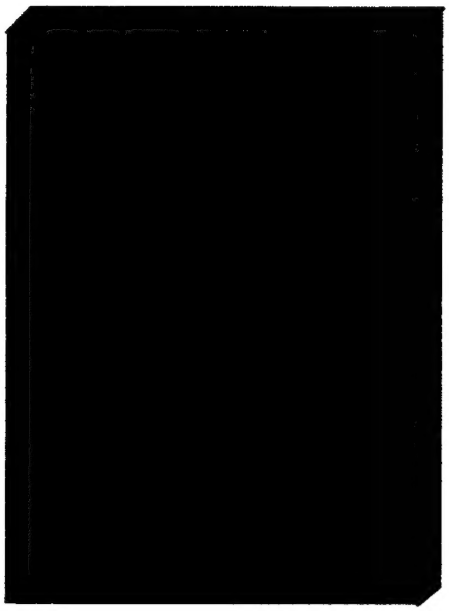


Figure 3: Shielded line and vertical transition for three-dimensional integration

To achieve high density in addition to very good performance in a three-dimensional circuit, vertical transitions characterized by small size, broad bandwidth and very low insertion loss are desired. As indicated on Figure 3, these transitions will facilitate the three-dimensional integration and will allow for new circuit architectures.

Circuit Power Combining - Corporate Feeding



- Offers:
  - Uniform amplitude and phase
  - A host of layout opportunities
- Suffers from:
  - Low Combining Efficiencies due to Loss from excessive line lengths
- ***Solution:***

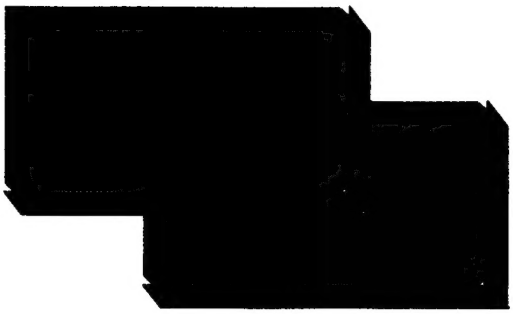
  3 Dimensional Corporate Feed Provides a Multitude of Architectures and has the Potential to Provide the Highest Combining Efficiency

Figure 4: Example of a corporate feed for a W-Band spatial combining network

Figures 4, 5 and 6 show a circuit schematic that illustrates the use of such a transition. In this transition development the challenge lies in the fabrication due to the requirement to photolithographically define lines on the side walls of the wafer. Our effort during the reporting period has resulted in the successful fabrication of these lines and has made the development of such transitions possible (see Figure 7). Presently we are in the process of fabricating these transitions within a circuit environment. These circuits will be measured for performance within the next two months.

State of the Art in Vertical Transitions

Metal Contact



Electromagnetic Transition

Most recent developments in vertical transitions
*** give 0.3-0.5 dB of return loss per transition**
*** high fabrication complexity**

Figure 5: State of the art in vertical transitions

3D Corporate Feed Structure

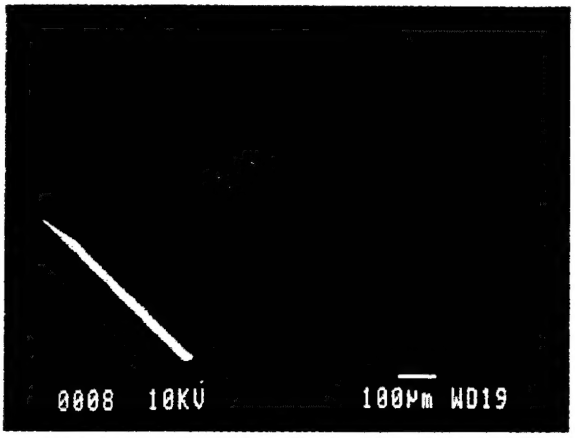
Three-dimensional integration :

- provides circuits of considerably reduced volume
- allows for a large variety of circuit architectures
- requires effective transition through multiple layers with much lower loss than state of the art
- requires high isolation for close proximity

Proposed Micromachined Transition is Expected to have insertion loss less than 0.1 dB

Figure 6: Proposed transition

Proposed Micromachined Vertical Transition



- **Conventional "spin-on" resist fails to provide adequate coverage**
- **Electrodepositable resist can uniformly coat high aspect ratio structures**
- **Diffraction effects (mask-to-cavity separation) during UV exposure hinders resolution → mask compensation can mitigate these effects**

Planar Transmission line patterned in 100 µm deep cavities.

Figure 7: Fabricated vertical transition

Brief Discussion of Future Work

A low noise amplifier/power amplifier pair will be fabricated and tested to demonstrate the application of integrated conformal packaging to very high density vertically integrated, three-dimensional MMIC circuits. The amplifier pair will use InP low noise and power HEMTs which will be bonded to the Si MMIC circuit using flip-chip techniques. The vertically integrated packaged amplifier pair will be designed to demonstrate 30dB gain and less than 2 dB noise figure at 20 and 32 GHz. The goal of this task is to demonstrate that Si micromachining can be implemented successfully to provide unprecedented circuit density combined with optimal performance, very small size and very low cost. Furthermore, this effort will indicate that high-resistivity silicon substrates have the best potential in overall system integration compared to GaAs, InP or any other substrate. The concept of integrated conformal packaging was first introduced by Drayton and Katehi in 1993. It is based on the architecture of the shielded coplanar waveguide (CPW) which is illustrated in Figure 3. The transmission line maintains all of the advantages of open CPW, such as uniplanar processing and ease of integration with two- and three-terminal active devices, with the added performance benefits of low radiation losses and reduced parasitic coupling to neighboring

components. Both fully shielded and half shielded lines have been studied and have shown performance advantages. These conformal packaged circuits will be used to realize the proposed amplifier pair. The amplifier/pair will be designed using high electron mobility transistors developed by Hughes Research Laboratories for low noise and high power performance respectively. The InP HEMT structure comprises a 250nm undoped AlInAs buffer with a 40nm GaInAs channel, a 1.5nm undoped spacer, an 8nm AlInAs donor layer, and a 7nm GaInAs doped cap. The material is grown by molecular beam epitaxy (MBE) and is lattice-matched to an InP semi-insulating substrate. The device is passivated with a 100 nm silicon nitride layer which causes some performance degradations.

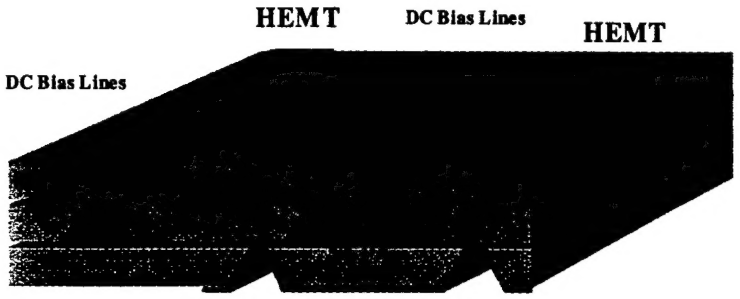


Figure 8: Proposed architecture for LNS/SSPA pair

The flip-chip transistor package is approximately 600 x 600 x 600mm3 in size and is mounted on the amplifier circuit via tin/lead solder bumps which have been electroplated on the transistor contact pads. The solder bumps are 25mm high and 50mm in diameter, and are reflowed to provide electrical contact to the amplifier As it has been discussed earlier, the design of the amplifier/pair circuit will be performed using finite ground coplanar waveguide lines. The total width (s+2w) of the lines will be selected to be 200mm to provide a convenient interface to the gate and drain pad dimensions of the HEMTs (see Figure 8). Results on this effort will be included in the next report.